WHAT IS CLAIMED IS:

1. An integrated circuit package having an array of metal pegs connected by printed circuit lines, comprising:

a die pad having a first surface and a second surface;

a die on the first surface of the die pad;

an insulating material that encloses the die and the die pad and exposes the second surface of the die pad;

a plurality of first metal pegs buried inside the insulating material and positioned around the die, with one end of each first metal peg embedded within the insulating material, and also electrically connected to the die;

a plurality of second metal pegs on the same side as the second surface of the die pad and positioned around the die pad;

a plurality of printed circuit lines on the same side as the second surface of the die pad, each printed circuit line located between a first metal peg and a second metal peg for connecting the two metal pegs electrically; and

a plurality of masks over the surfaces of the printed circuit lines.

2. The integrated circuit package of claim 1, wherein the die pad, the first metal pegs and the second metal pegs are made from one of the materials including copper, copper alloy, iron or iron alloy.

3. The integrated circuit package of claim 1, wherein the end face of each first metal peg buried inside the insulating material contains a first electroplate layer.

4. The integrated circuit package of claim 3, wherein the first electroplate layer is made from a material chosen from a group consisting of gold, silver, nickel, palladium and a combination of them.

5. The integrated circuit package of claim 1, wherein the end face of each second metal peg contains a second electroplate layer.

6. The integrated circuit package of claim 5, wherein the second electroplate layer is a material chosen from a group consisting of gold, silver, nickel, palladium and a combination of them.

7. The integrated circuit package of claim 1, wherein the mask is made from an insulating paint that is capable of being thermally hardened.

8. The integrated circuit package of claim 1, wherein a plurality of conductive wires is used for electrically connecting the die to the first metal pegs.

9. The integrated circuit package of claim 8, wherein the conductive wires include gold wires.

10. The integrated circuit package of claim 1, wherein the insulating material includes resin.

11. The integrated circuit package of claim 1, wherein the insulating material includes epoxy.

12. The integrated circuit package of claim 5, wherein a solder ball is further attached to each second electroplate layer.

13. The integrated circuit package of claim 5, wherein a copper ball is further attached to each second electroplate layer.

14. The integrated circuit package of claim 5, wherein a solder paste layer is further smeared onto each second electroplate layer.

15. A method for forming an integrated circuit package that contains an array of metal pegs connected by printed circuit lines, comprising the steps of:

providing a metal substrate that has a first surface and a second surface;

forming a plurality of first electroplate layers on the first surface and forming a plurality of second electroplate layers on the second surface;

forming a mask layer over the first surface to form a die pad region so that the first electroplate layers are positioned around the die pad region;

etching the exposed metal substrate on the first surface using the mask layer and the first electroplate layers as an etching mask to form a die pad and a plurality of first metal pegs;

removing the mask layer;

attaching a silicon die over the die pad, and connecting the die and the first electroplate layers electrically, wherein area of the die pad region is smaller than the area of the die;

enclosing the die, the die pad, the first electroplate layers and the first metal pegs above the first surface of the metal substrate with an insulating material;

forming a plurality of circuit line masks on the second surface of the metal substrate; and

etching the exposed metal substrate on the second surface using the second electroplate layers and the circuit line mask as an etching mask to from a plurality of second metal pegs and a plurality of printed circuit lines.

16. The method of claim 15, wherein the step of forming the first electroplate layers and the second electroplate layers further includes:

forming a first photoresist layer and a second photoresist layer over the first surface and the second surface of the metal substrate, respectively;

carrying out exposure and development operations with regards to the first and the second photoresist layers, respectively, so that a portion of the first surface and a

portion of the second surface are exposed, thus defining a plurality of first metal pegs regions and a plurality of second metal pegs regions; and

conducting an electroplating operation to form first electroplate layers and second electroplate layers over the first metal peg regions and the second metal peg regions, respectively.

17. The method of claim 16, wherein after the step of forming the first electroplate layers and the second electroplate layers, but before the step of forming the mask layer, further includes removing the first photoresist layer.

18. The method of claim 15, wherein the step of forming the first electroplate layers includes electroplating a material chosen from a group consisting of gold, silver, nickel, palladium and a combination of them.

19. The method of claim 15, wherein the step of forming the second electroplate layer includes electroplating gold, silver, nickel, palladium or a combination of them.

20. The method of claim 15, wherein the step of forming the mask layer includes:

forming a photoresist layer over the first surface of the metal substrate; and

exposing the photoresist layer and developing the photoresist layer to form the mask layer.

21. The method of claim 15, wherein the step of forming the circuit line masks includes using a screen printing method.

22. The method of claim 15, wherein after the step of forming the printed circuit lines, further includes forming a plurality of sidewall masks on the sidewalls of the circuit lines.

23. The method of claim 22, wherein the step of forming the sidewall masks includes using a screen printing method.

24. The method of claim 15, wherein after the step of forming the printed circuit lines, further includes attaching a solder ball to the surface of each second electroplate layer.

25. The method of claim 15, wherein after the step of forming the printed circuit lines, further includes attaching a copper ball to the surface of each second electroplate layer.

26. The method of claim 15, wherein after the step of forming the printed circuit lines, further includes smearing solder paste over the surface of each second electroplate layer.